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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,478	10/01/2003	Shibly S. Ahmed	H1487	4674
45114	7590	04/18/2005	EXAMINER	
HARRITY & SNYDER, LLP 11240 WAPLES MILL ROAD SUITE 300 FAIRFAX, VA 22030			BERRY, RENEE R	
			ART UNIT	PAPER NUMBER
			2818	
DATE MAILED: 04/18/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/674,478

Applicant(s)

AHMED ET AL.

Examiner

Renee R. Berry

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 January 2005.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6-8, and 16-19 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4, 6-8 and 16-19 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 01 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6-8, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,764,884 to Yu et al. in view US Patent No. 6,699,758 to Hirano et al.

In regards to claim 1, Yu teaches a semiconductor device, comprising: a substrate; an insulating layer formed on the substrate; a fin formed on the insulating layer; silicided source and drain regions formed adjacent the fin; and a metal gate formed over a portion of the fin at column 7, lines 62-67 to column 8, lines 1-21 and lines 37-40.

In regards to claim 2, Yu teaches the semiconductor device of claim 1 wherein fin includes silicon at column 7, lines 65-66.

In regards to claim 3, Yu teaches the semiconductor device of claim 1, wherein the metal gate includes tantalum or titanium at column 10, lines 17-18.

In regards to claim 4, Yu teaches the semiconductor device of claim 1, further comprising: at least one dielectric layer formed between the fin and the metal gate at column 10, lines 6-7.

In regards to claim 6, Yu teaches the semiconductor device of claim 5, wherein the silicided source and drain regions have a thickness ranging from about 400 Å to about 1500 Å at column 4, lines 30-34.

In regards to claim 7, Yu teaches the semiconductor device of claim 1, further comprising: a pair of spacers formed over portions of the fin and on opposite sides of the metal gate at column 8, lines 22-25.

In regards to claim 8, Yu teaches the semiconductor device of claim 7, wherein the portions of the fin under the pair of spacers separate a channel region of the fin from the silicided source and drain regions at column 8, lines 37-40.

In regards to claim 16, Yu teaches a semiconductor device, comprising: a substrate; an insulating layer formed on the substrate; a fin formed on the insulating layer; a dielectric layer formed on the fin; a metal gate formed over a portion of the fin and the dielectric layer; a pair of spacers formed on the fin on opposite sides of the metal gate; and formed on the opposite sides of the metal gate at column 7, lines 62-67 to column 8, lines 1-21 and lines 37-40.

In regards to claim 17, Yu teaches the semiconductor device of claim 16, wherein the metal gate includes tantalum or titanium at column 10, lines 17-19.

In regards to claim 18, Yu teaches the semiconductor device of claim 16, wherein the silicided source and drain regions are composed of silicide down to the insulating layer at column 8, lines 37-40.

Art Unit: 2829

In regards to claim 19, Yu teaches the semiconductor device of claim 16, wherein the metal gate and the wherein the silicided source and drain regions comprise a silicide material down pair of spacers are located over a channel region of the fin, and to the insulating layer at column 8, lines 22-24.

However, Yu does not teach all the limitations of the following claims:

In regards to claim 1, Hirano teaches the silicided source and drain regions are silicided down to the insulating layer at column 1, lines 56-60.

In regards to claim 16, Hirano teaches silicided source and drain regions having a thickness ranging from about 400 Angstroms to about 1500 Angstroms at column 11, lines 11-15, Figure 23, reference numbers 71 and 72.

Therefore, it would have been obvious to one having ordinary skill in the art to have modified Yu to include the silicided source and drain regions are silicided down to the insulating layer and silicided source and drain regions having a thickness ranging from about 400 Angstroms to about 1500 Angstroms, since such a modification would result in leakage current, as described in column 1, lines 60-64 of Hirano et al.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

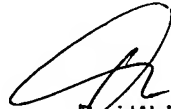
Art Unit: 2829

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



RRB

March 21, 2005



David Nelms  
Supervisory Patent Examiner  
Technology Center 2800